FIG. 1

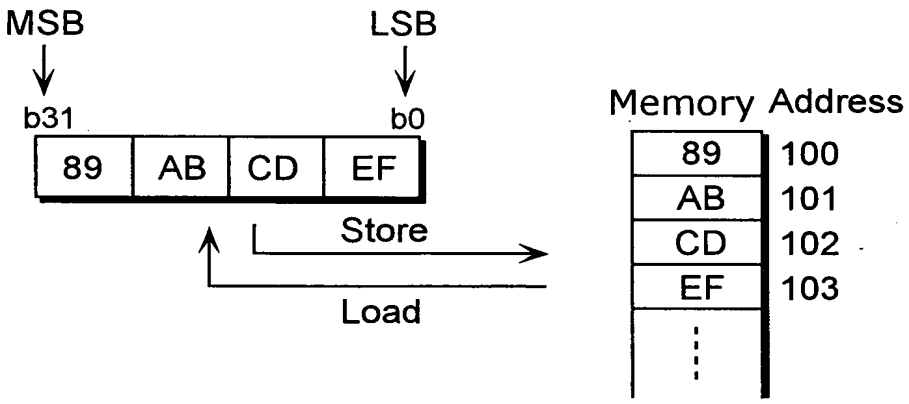
MSB
LSB
b31
b0
89
AB
CD
EF
Store
Load
Memory Address
89
AB
CD
EF
100
101
102
103

FIG. 2

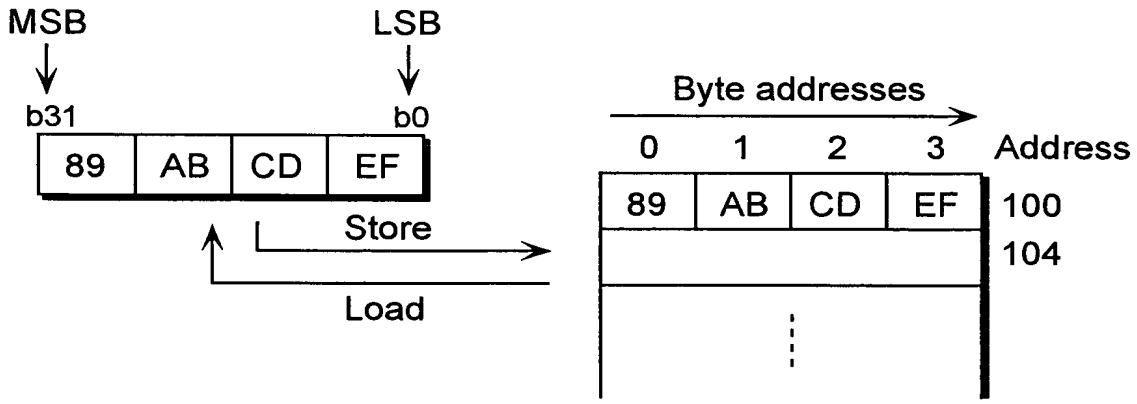
MSB
LSB
b31
b0
89
AB
CD
EF
Store
Load
Byte addresses
0
1
2
3
Address
89
AB
CD
EF
100
104

FIG. 3

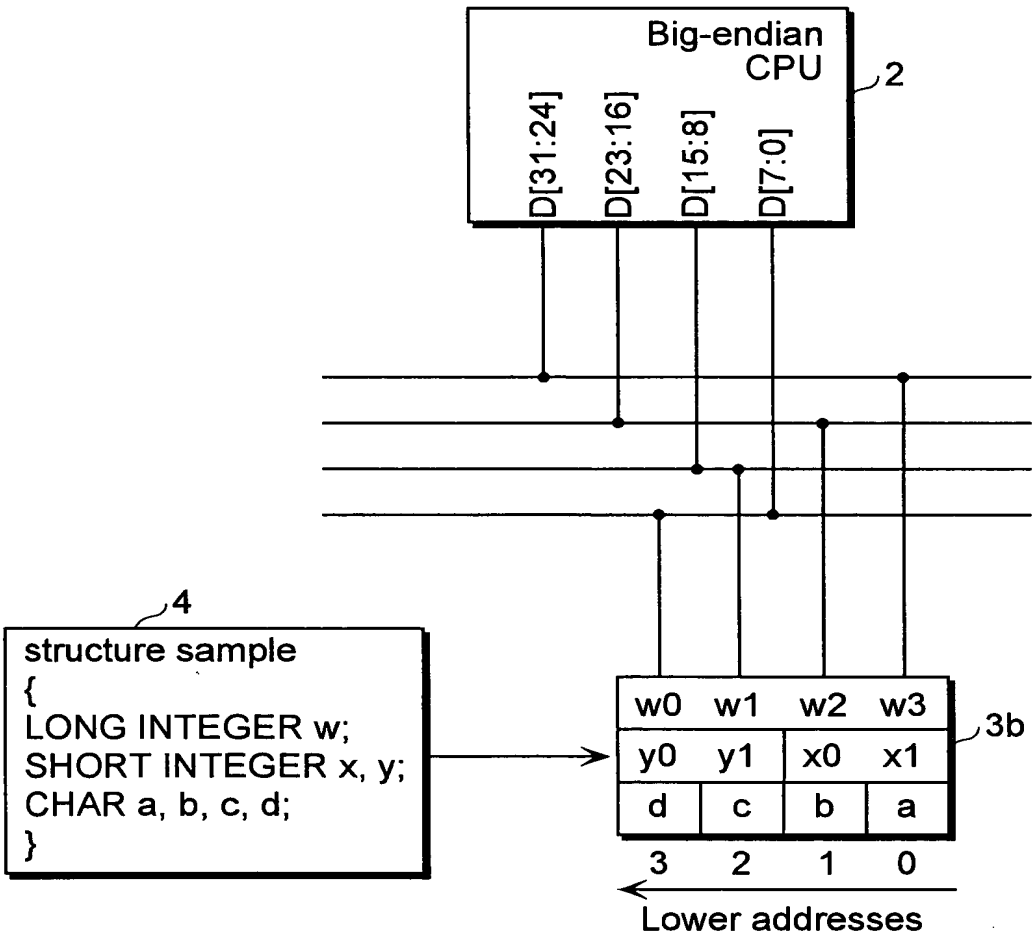
Big-endian CPU
2
D[31:24]
D[23:16]
D[15:8]
D[7:0]
4
structure sample
{
LONG INTEGER w;
SHORT INTEGER x, y;
CHAR a, b, c, d;
}
w0 w1 w2 w3
y0 y1 x0 x1
d c b a
3b
3 2 1 0
Lower addresses

FIG. 4

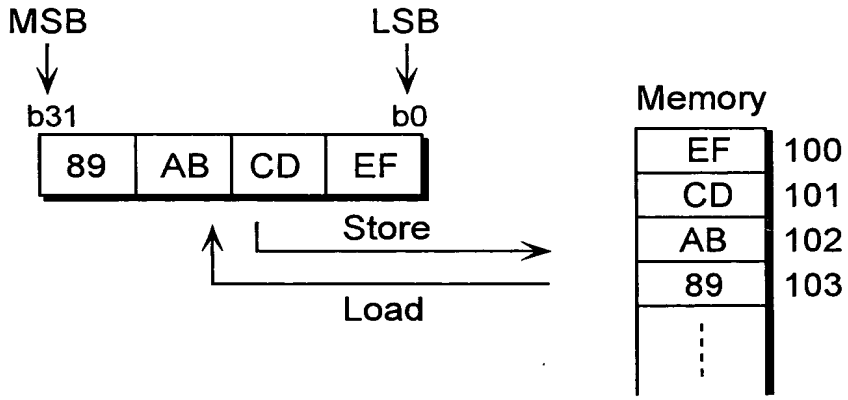
MSB
LSB
b31
b0
89
AB
CD
EF
Store
Load
Memory
EF
CD
AB
89
100
101
102
103

FIG. 5

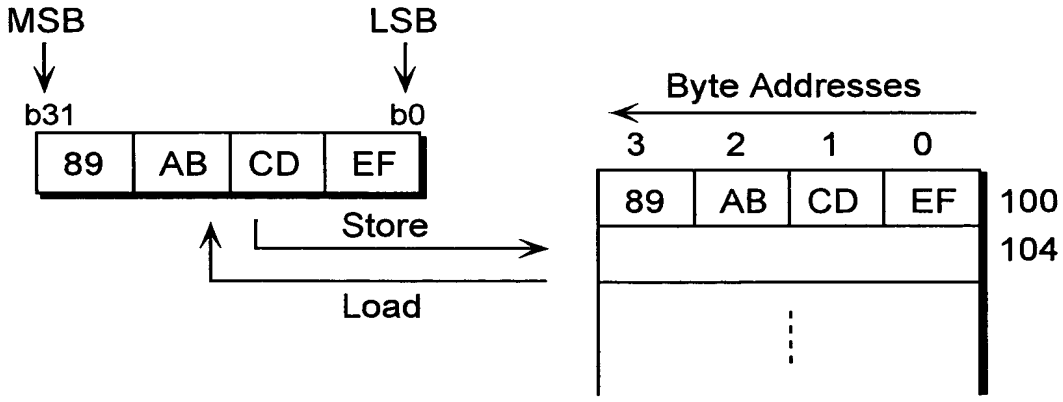
MSB
LSB
b31
b0
89
AB
CD
EF
Store
Load
Byte Addresses
3
2
1
0
89
AB
CD
EF
100
104

FIG. 6

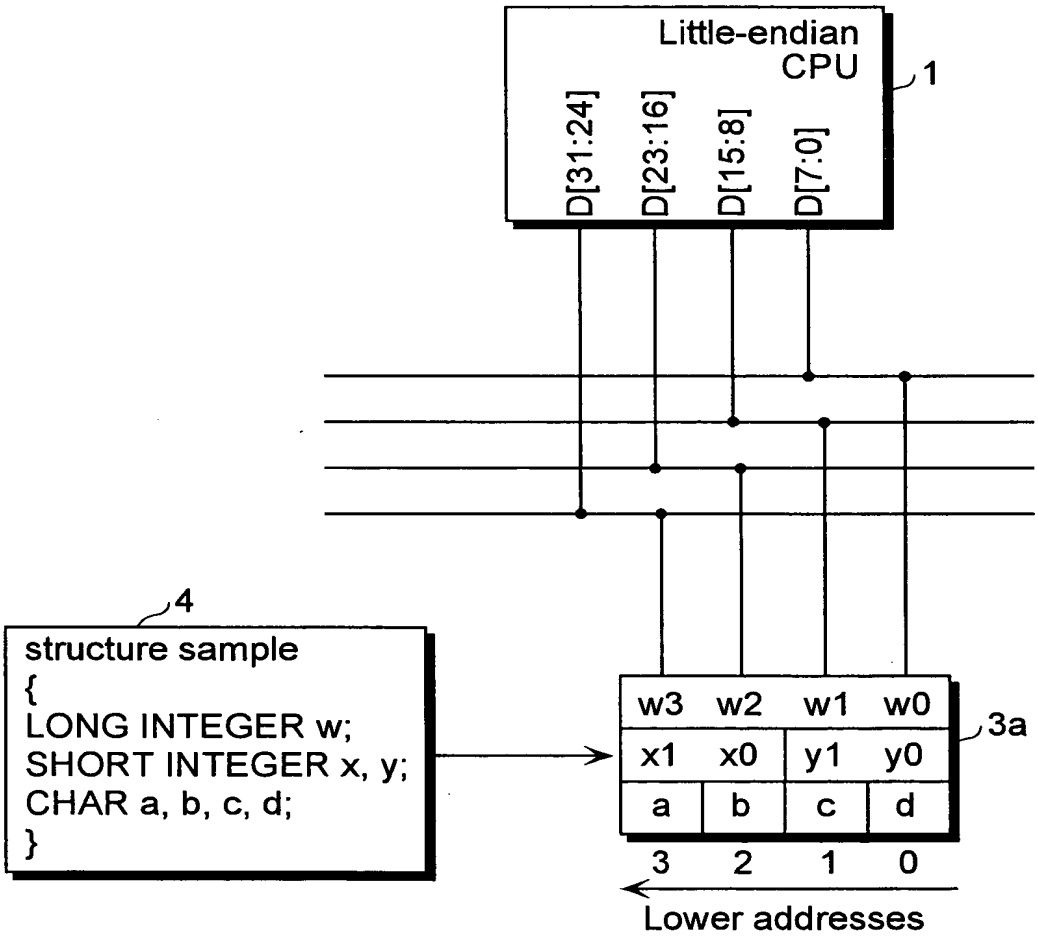
Little-endian CPU
1
D[31:24]
D[23:16]
D[15:8]
D[7:0]
4
structure sample
{
LONG INTEGER w;
SHORT INTEGER x, y;
CHAR a, b, c, d;
}
w3 w2 w1 w0
x1 x0 y1 y0
a b c d
3a
3 2 1 0
Lower addresses

FIG. 7

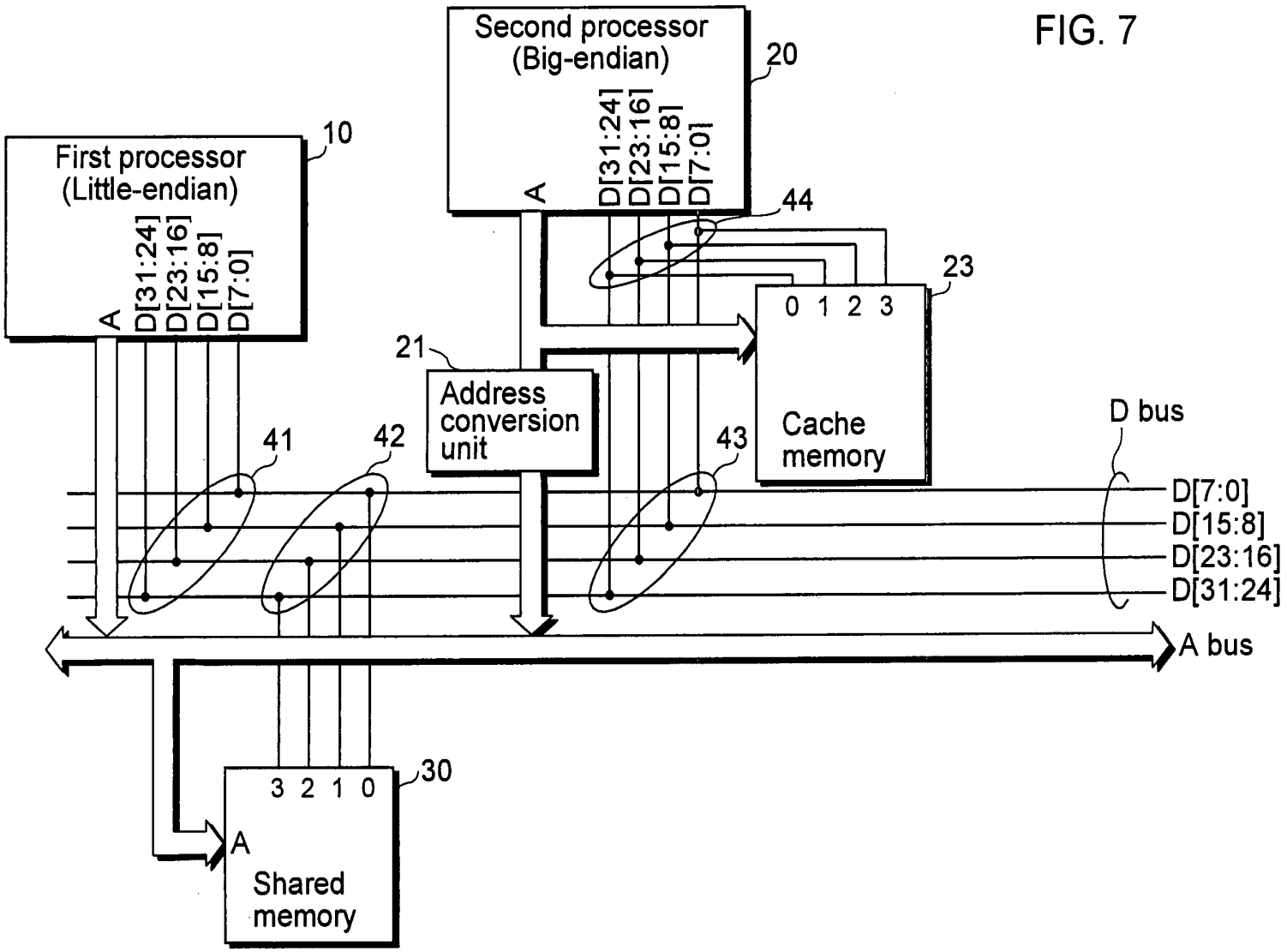
Second processor
(Big-endian)
20
A
D[31:24]
D[23:16]
D[15:8]
D[7:0]
First processor
(Little-endian)
10
A
D[31:24]
D[23:16]
D[15:8]
D[7:0]
44
23
0 1 2 3
21
Address
conversion
unit
Cache
memory
D bus
41
42
43
D[7:0]
D[15:8]
D[23:16]
D[31:24]
A bus
3 2 1 0
30
A
Shared
memory

FIG. 8

Input		Output
Access size	Address	Converted address
w (32 Bits)	A1, A0	A1, A0
hw (16 Bits)	A1, A0	$\overline{A1}$, A0
B (8 Bits)	A1, A0	$\overline{A1}$, $\overline{A0}$

FIG. 9

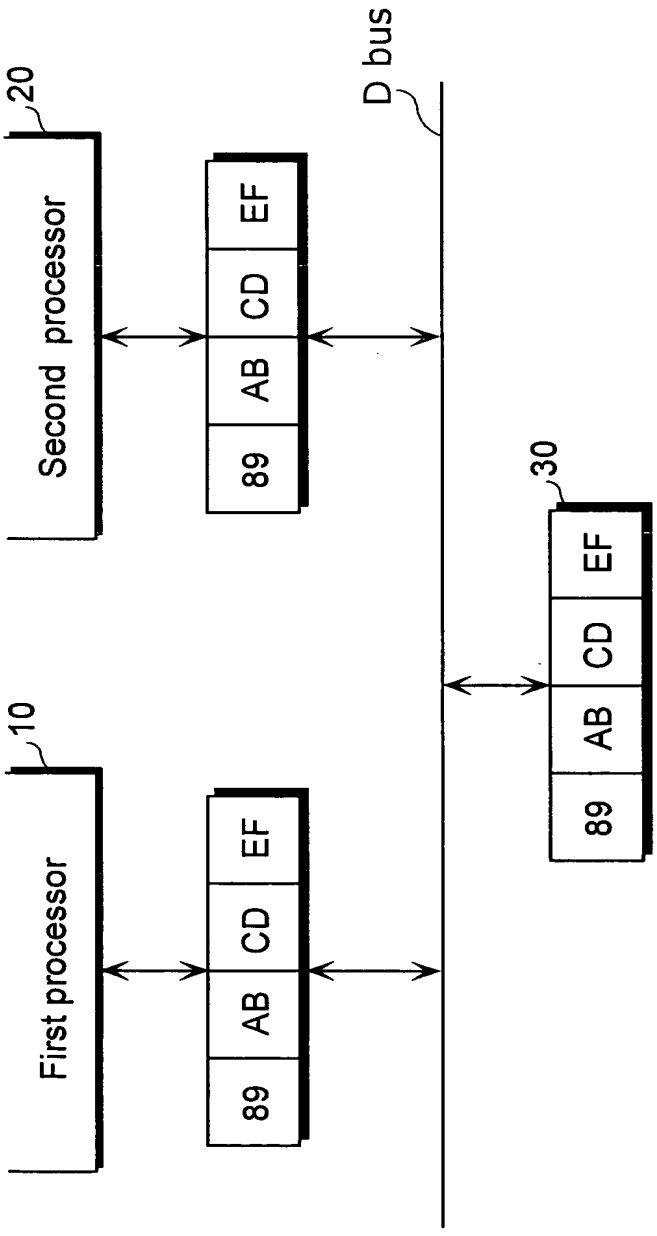
D bus
20
Second processor
89
AB
CD
EF
10
First processor
89
AB
CD
EF
30
89
AB
CD
EF

FIG. 10A

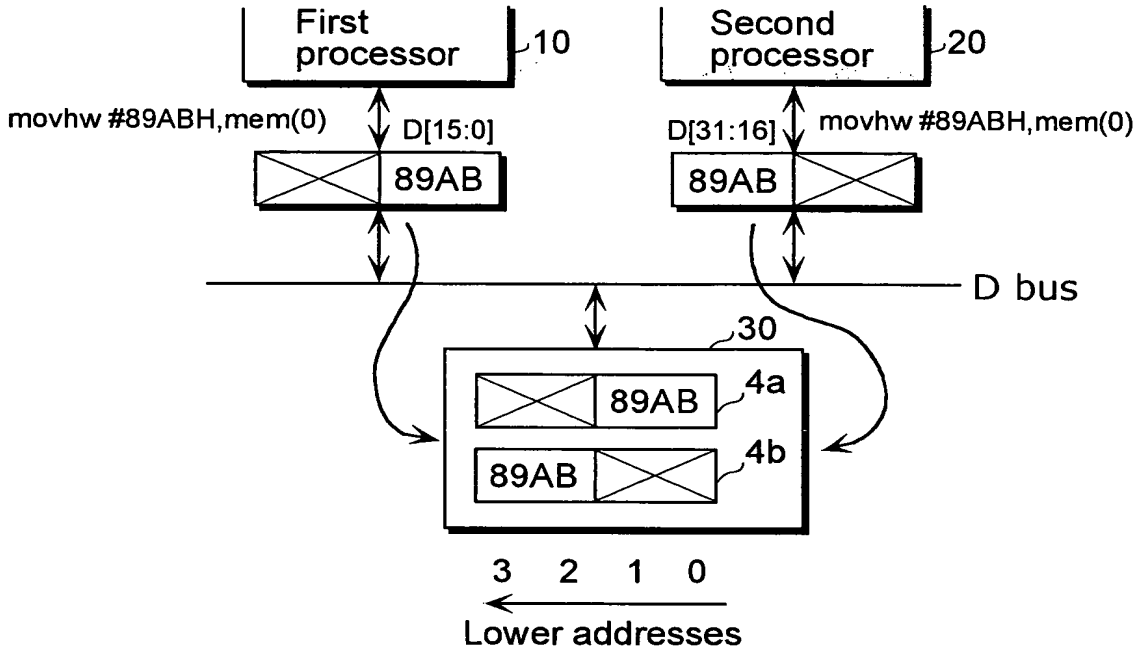

FIG. 10B

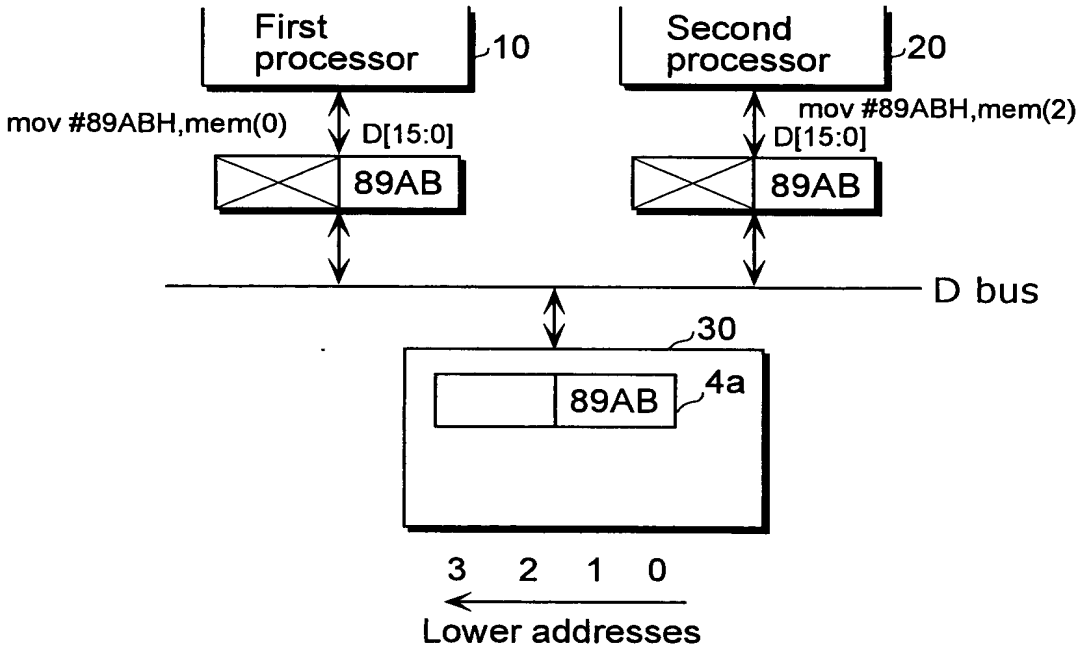

FIG. 11A

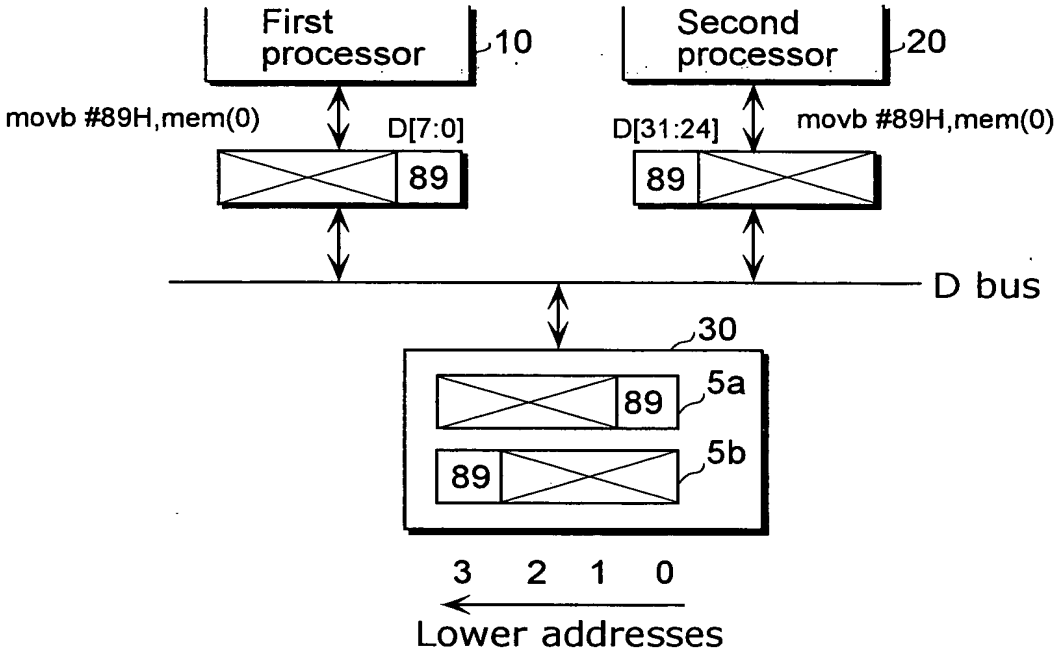

FIG. 11B

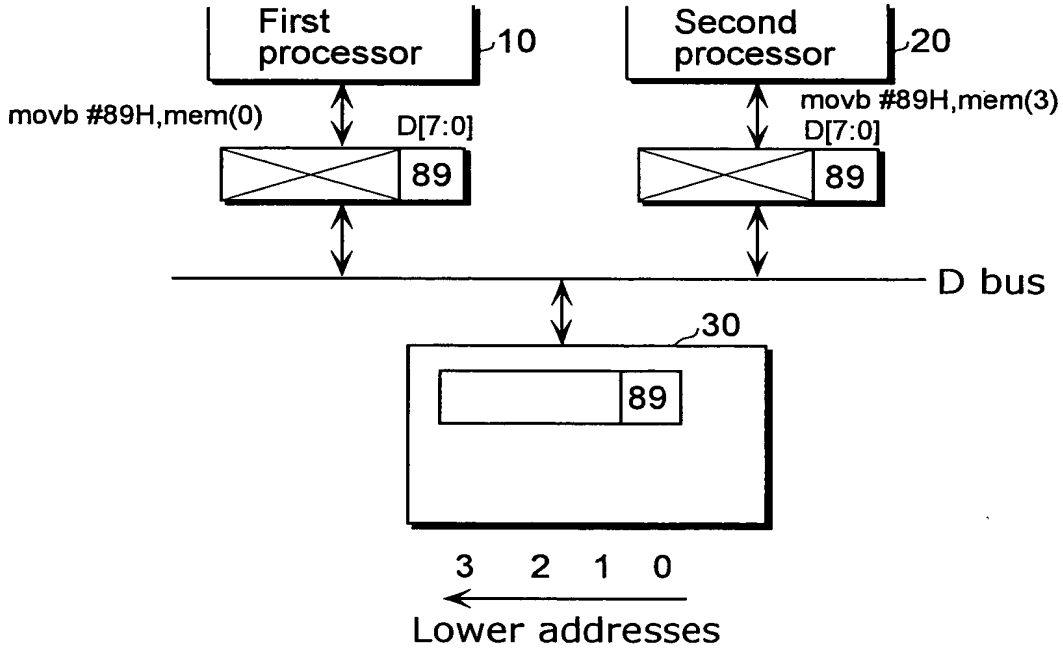

FIG. 12

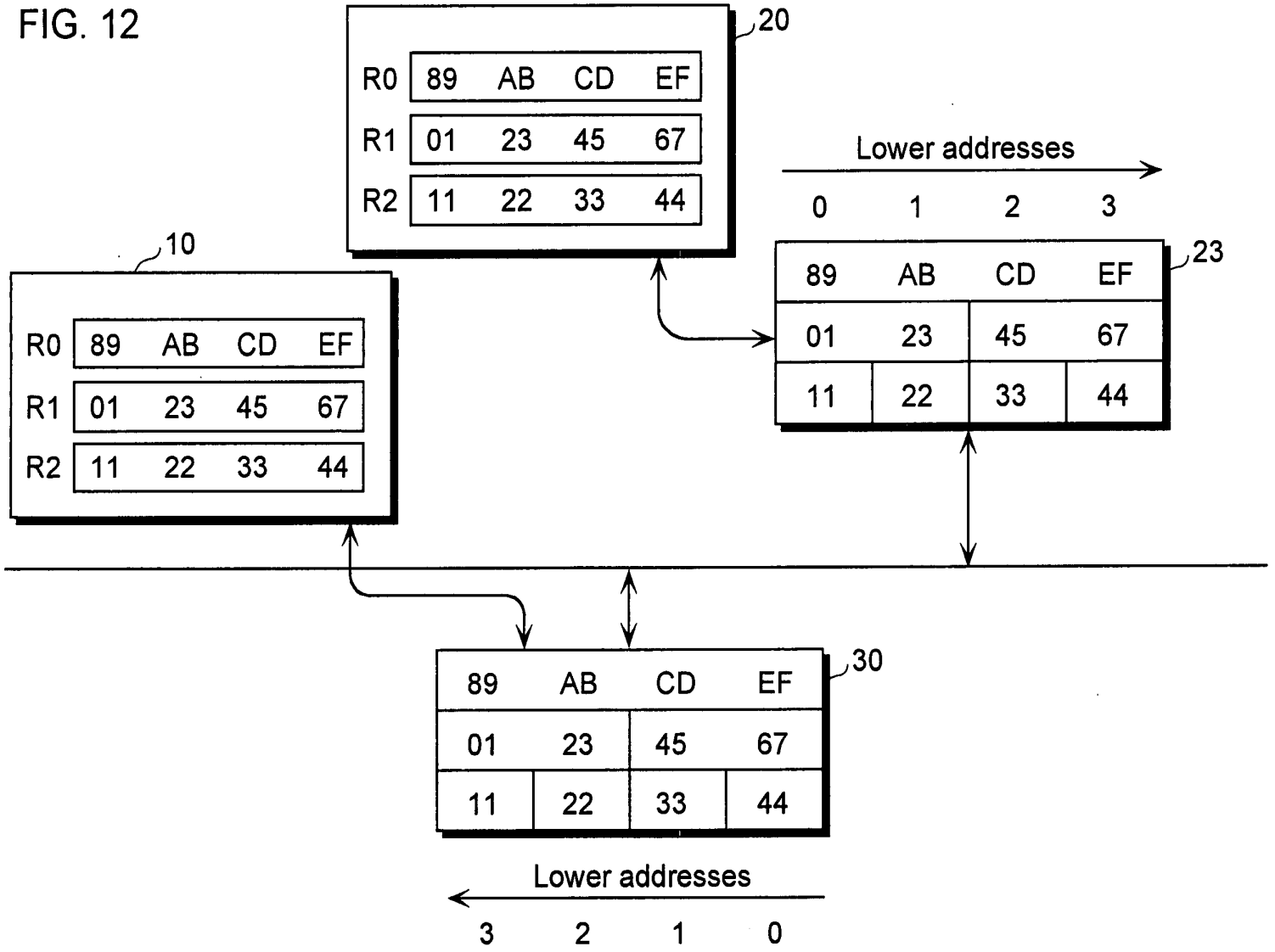
20
R0 89 AB CD EF
R1 01 23 45 67
R2 11 22 33 44
Lower addresses
0 1 2 3
23
89 AB CD EF
01 23 45 67
11 22 33 44
10
R0 89 AB CD EF
R1 01 23 45 67
R2 11 22 33 44
30
89 AB CD EF
01 23 45 67
11 22 33 44
Lower addresses
3 2 1 0

FIG. 13

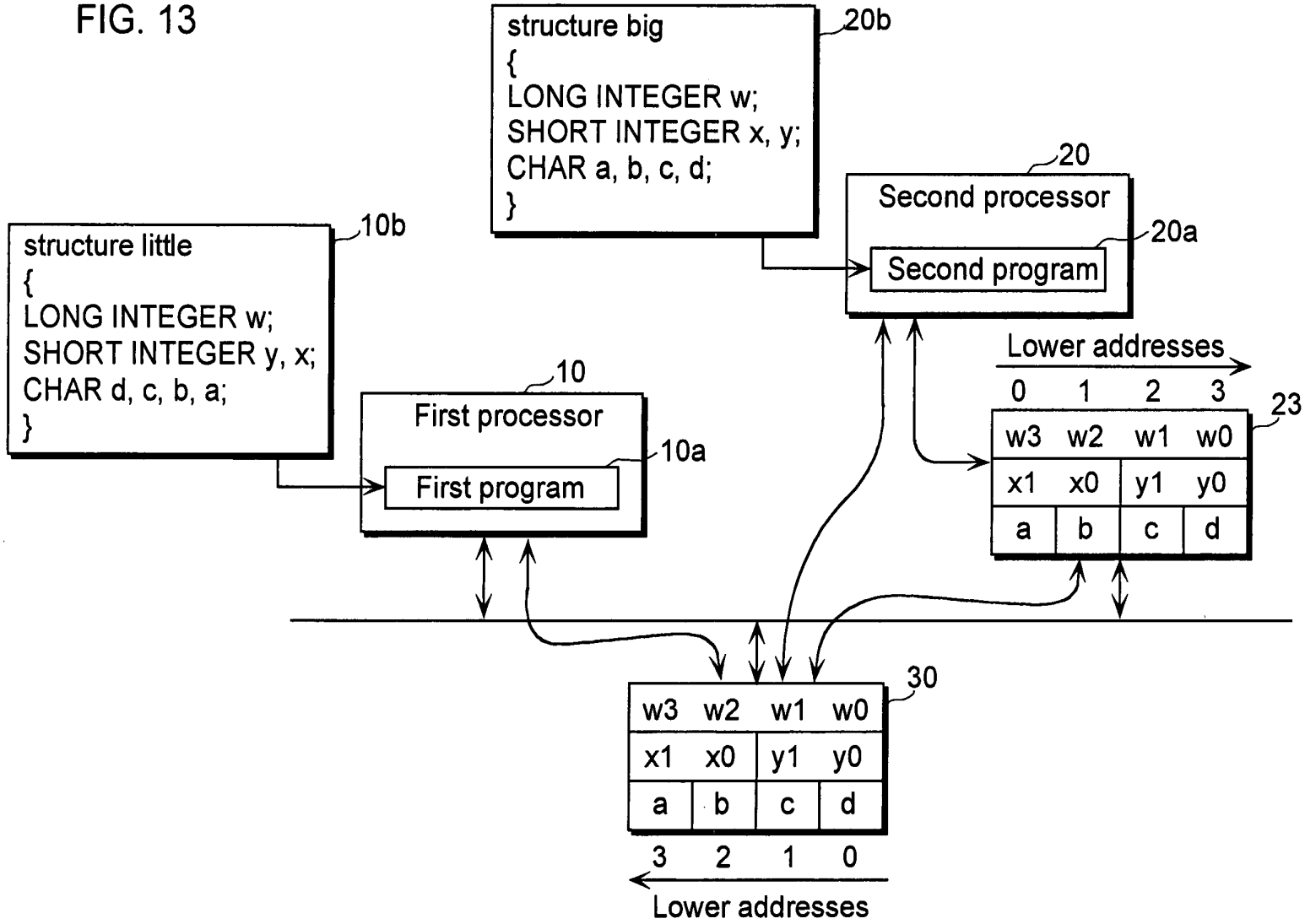
structure big
{
LONG INTEGER w;
SHORT INTEGER x, y;
CHAR a, b, c, d;
}
20b
20
Second processor
Second program
20a
structure little
{
LONG INTEGER w;
SHORT INTEGER y, x;
CHAR d, c, b, a;
}
10b
10
First processor
First program
10a
Lower addresses
0 1 2 3
23
w3 w2 w1 w0
x1 x0 y1 y0
a b c d
30
w3 w2 w1 w0
x1 x0 y1 y0
a b c d
3 2 1 0
Lower addresses

FIG. 14

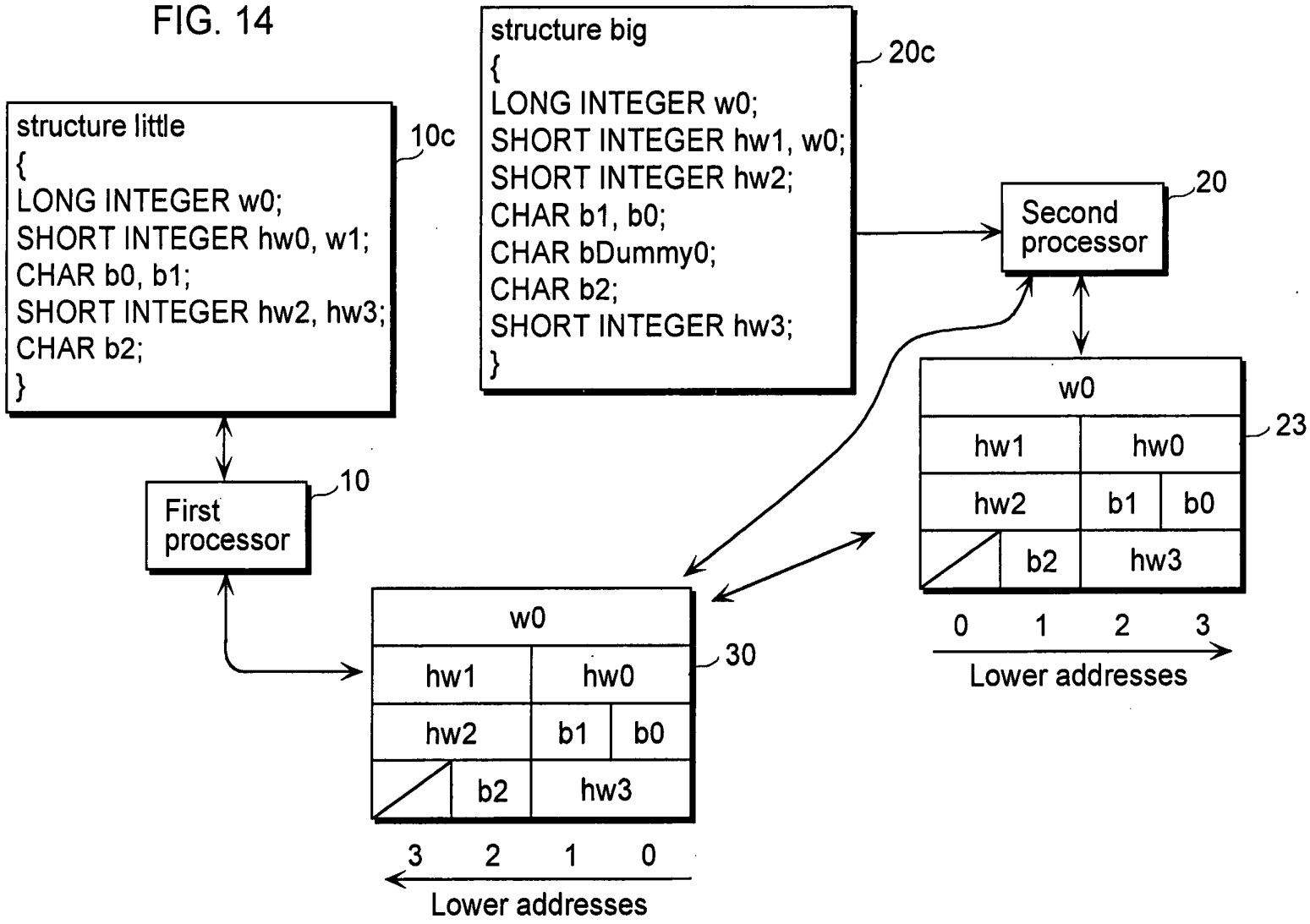
structure little
{
LONG INTEGER w0;
SHORT INTEGER hw0, w1;
CHAR b0, b1;
SHORT INTEGER hw2, hw3;
CHAR b2;
}
10c
structure big
{
LONG INTEGER w0;
SHORT INTEGER hw1, w0;
SHORT INTEGER hw2;
CHAR b1, b0;
CHAR bDummy0;
CHAR b2;
SHORT INTEGER hw3;
}
20c
First processor
10
Second processor
20
w0
hw1
hw0
hw2
b1
b0
b2
hw3
30
3 2 1 0
Lower addresses
23
0 1 2 3
Lower addresses

FIG. 15

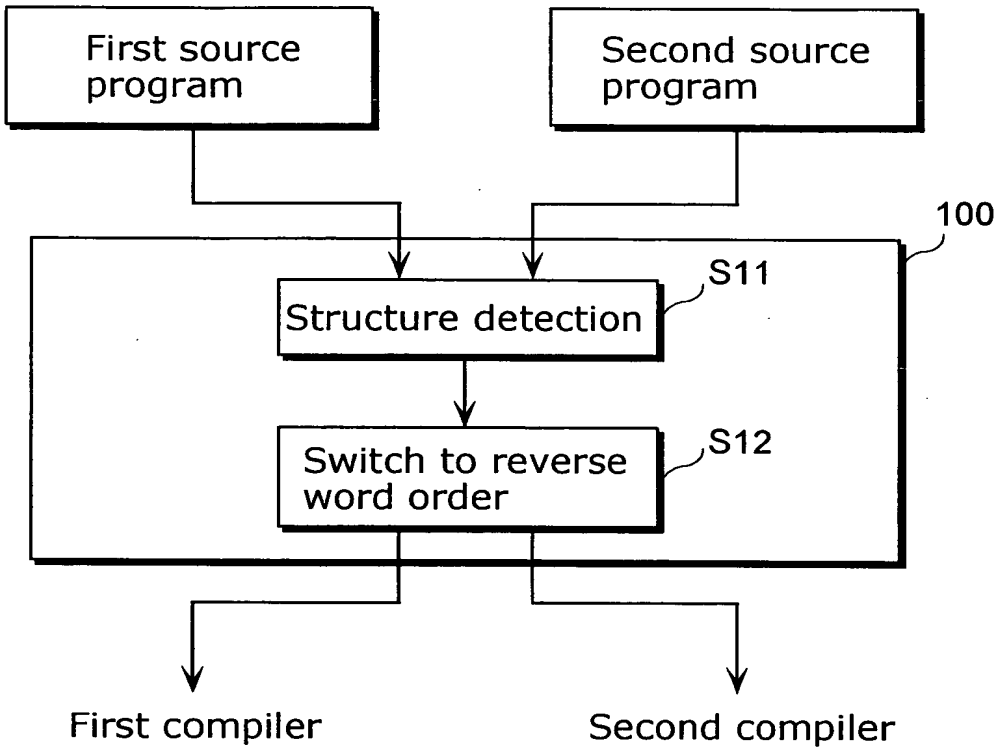
First source program
Second source program
100
S11
Structure detection
S12
Switch to reverse word order
First compiler
Second compiler

FIG. 16

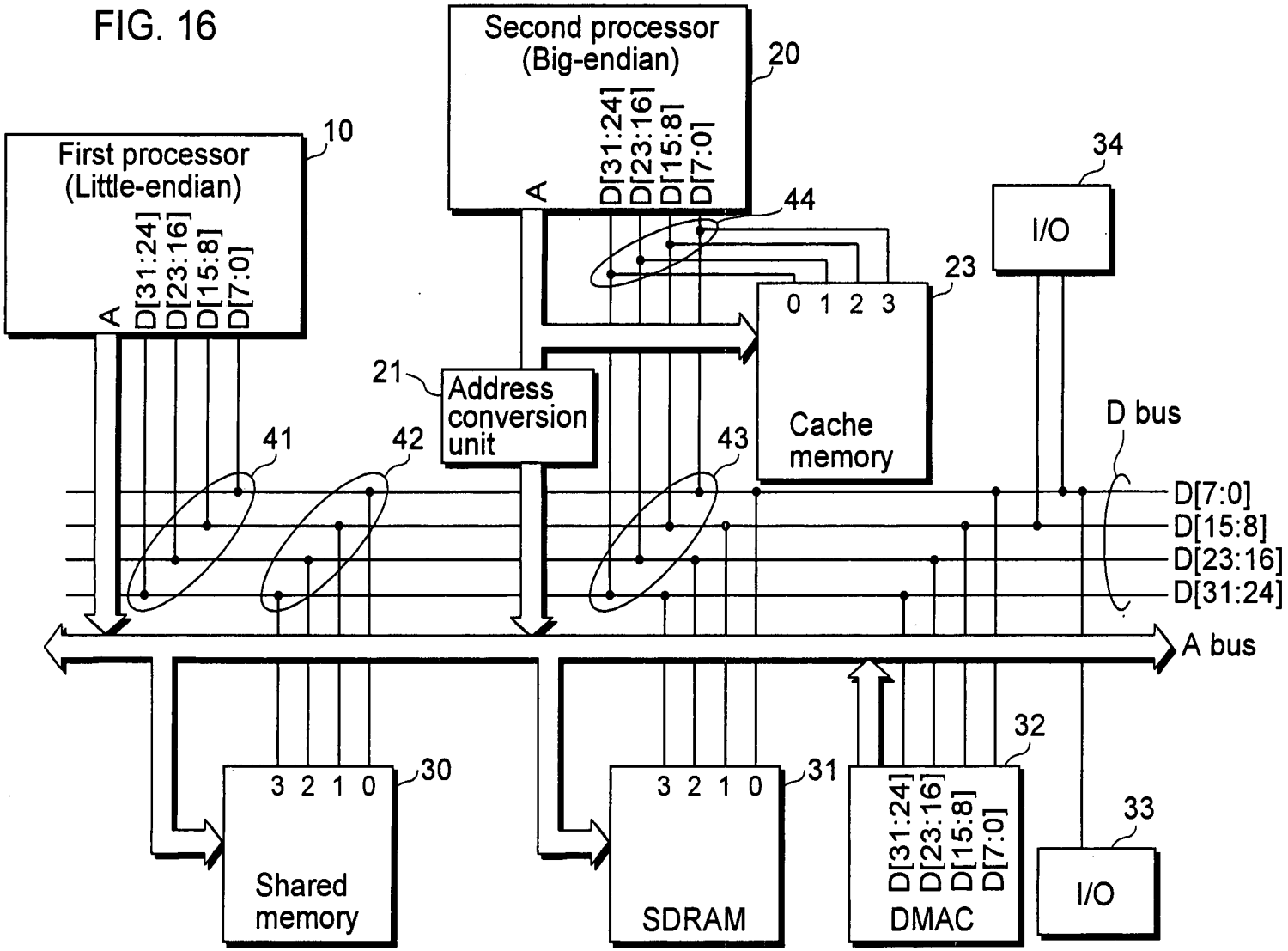
Second processor
(Big-endian)
20
A
D[31:24]
D[23:16]
D[15:8]
D[7:0]
First processor
(Little-endian)
10
A
D[31:24]
D[23:16]
D[15:8]
D[7:0]
34
I/O
44
23
0 1 2 3
Cache
memory
21
Address
conversion
unit
41
42
43
D bus
D[7:0]
D[15:8]
D[23:16]
D[31:24]
A bus
3 2 1 0
30
Shared
memory
3 2 1 0
31
SDRAM
32
D[31:24]
D[23:16]
D[15:8]
D[7:0]
DMAC
33
I/O

FIG. 17

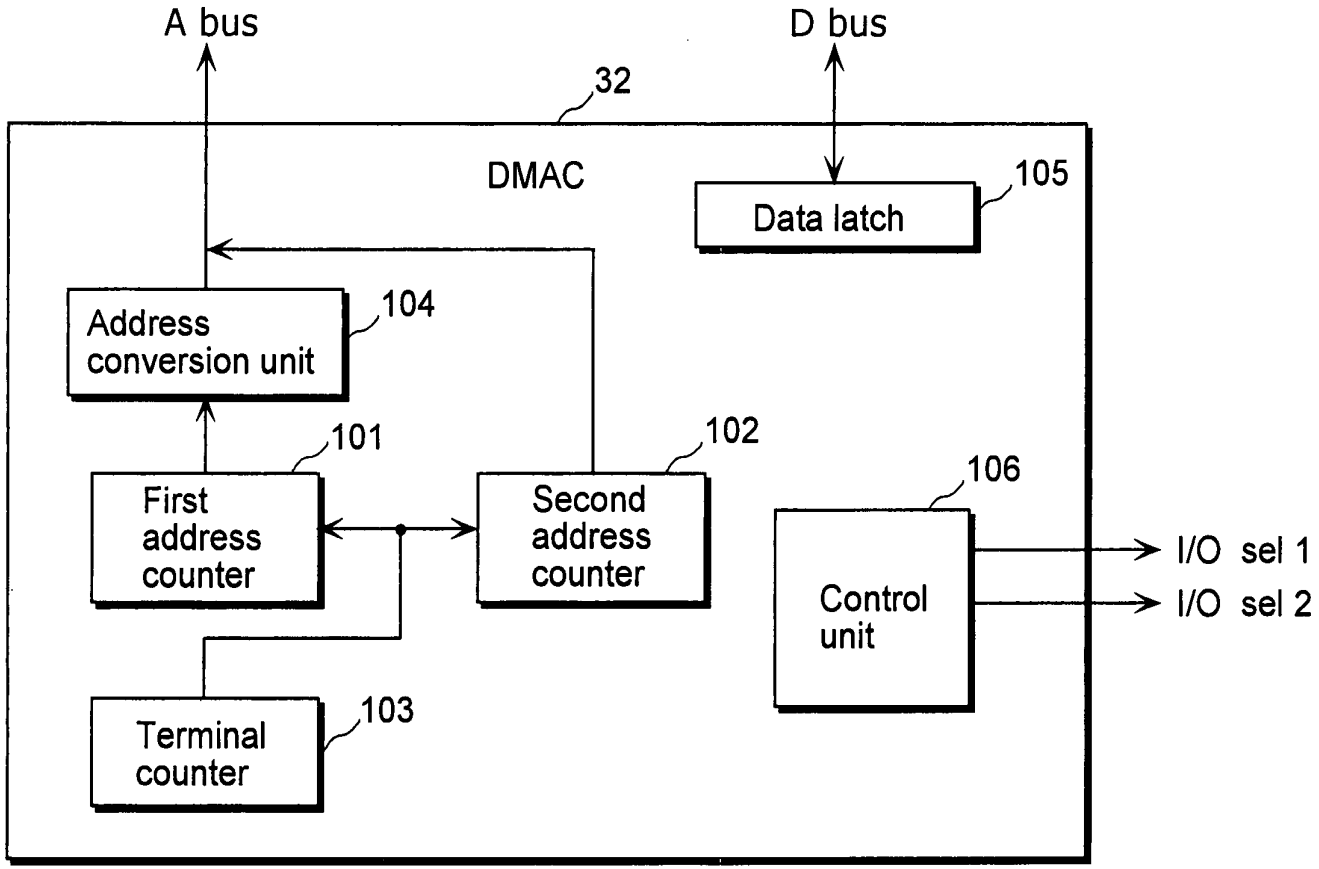
A bus
D bus
32
DMAC
Data latch
105
Address conversion unit
104
101
First address counter
102
Second address counter
106
Control unit
I/O sel 1
I/O sel 2
Terminal counter
103

FIG. 18

Input			Output
Endian	Access size	Address	Converted address
Same	X	A1, A0	A1, A0
Different	w (32 Bits)	A1, A0	A1, A0
Different	hw (16 Bits)	A1, A0	$\overline{A1}$, A0
Different	b (8 Bits)	A1, A0	$\overline{A1}$, $\overline{A0}$

FIG. 19A

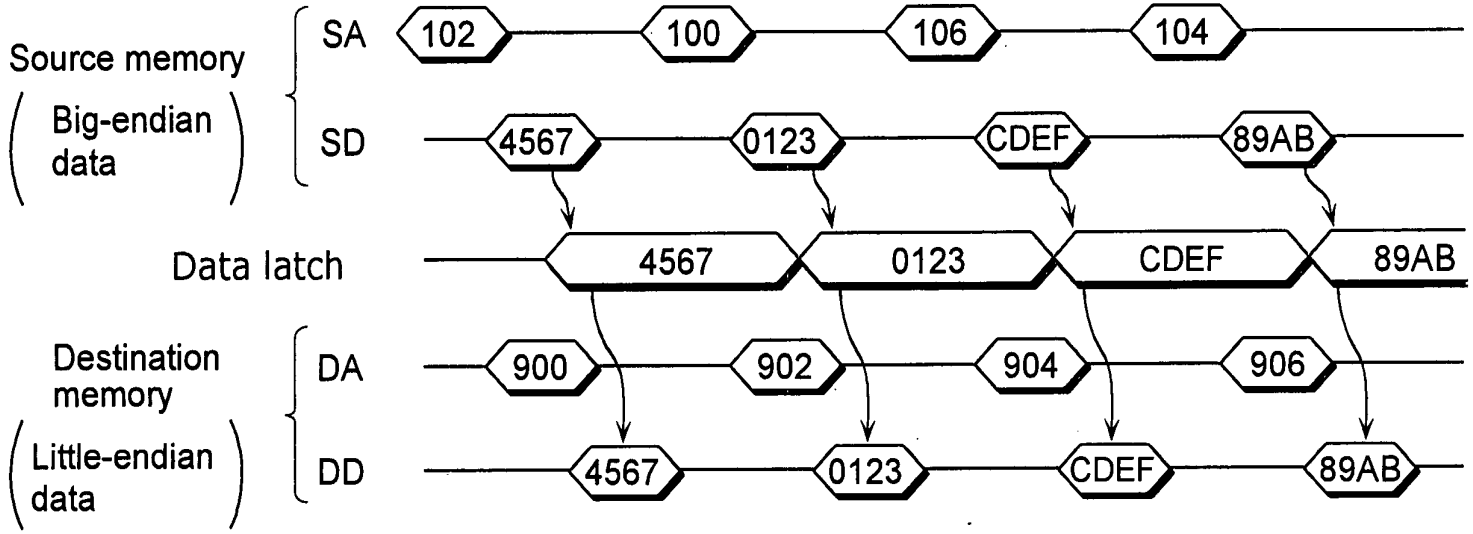

FIG. 19B